

**NON-VOLATILE MEMORY CELL COMPRISING DIELECTRIC LAYERS HAVING
A LOW DIELECTRIC CONSTANT AND CORRESPONDING
MANUFACTURING PROCESS**

ABSTRACT

5 A non-volatile memory cell is described, being integrated on a semiconductor substrate and comprising: A floating gate transistor including a source region and a drain region, a gate region projecting from the substrate and comprised between the source and drain regions, the gate region having a predetermined length and width and comprising a first floating gate region and a control gate region, in which
10 the floating gate region is insulated laterally, along the width direction, by a dielectric layer with low dielectric constant value. A process for manufacturing non-volatile memory cells on a semiconductor substrate is also described, comprising the following steps: form active areas in the semiconductor substrate bounded by an insulating layer, deposit a first conductor material layer on active areas, define
15 through a standard photolithographic technique a plurality of floating gate regions, form a dielectric layer with low dielectric constant value on the floating gate regions.